REMARKS

Applicants respectfully request reconsideration of the present application in view of the foregoing amendments and in view of the reasons that follow.

Status of Claims:

No claims are currently being cancelled.

Claims 1, 6, 7, 9, 13 and 18 are currently being amended.

No claims are currently being added.

This amendment and reply amends claims in this application. A detailed listing of all claims that are, or were, in the application, irrespective of whether the claims remain under examination in the application, is presented, with an appropriate defined status identifier.

After amending the claims as set forth above, claims 1-3, 6-12 and 18-20 are pending in this application for examination on the merits, whereby claims 13-17 are withdrawn from consideration as being directed to a non-elected species.

Claim Rejections – Written Description:

In the final Office Action, claims 6 and 18 were rejected under 35 U.S.C. § 112, 1st paragraph, as failing to comply with the written description requirement, for the reasons set forth on pages 2 and 3 of the Office Action. By way of this amendment and reply, claim 6 has been amended to remove the language in that claim that was alleged to lack sufficient written description support. With respect to claim 18, that claim has also been amended to remove the language in that claim that was alleged to lack sufficient written description support in order to expedite prosecution. In view of this amendment, it should be clear that the CPU 2 is directly connected to the memory controller 18, as seen in Figure 1 of the drawings, for example.

Accordingly, presently pending claims 6 and 18 are believed to fully comply with 35 U.S.C. § 112, 1st paragraph.

Claim Rejections – Indefiniteness:

In the final Office Action, claims 1 and 6 were rejected under 35 U.S.C. § 112, 2nd paragraph, as being indefinite, for the reasons set forth on pages 3 and 4 of the Office Action. By way of this amendment and reply, claims 1 and 6 have been amended to address the 'indefiniteness' issues raised in the Office Action. Accordingly, presently pending claims 1 and 6 are believed to fully comply with 35 U.S.C. § 112, 2nd paragraph.

Claim Rejections – Prior Art:

In the Office Action, claims 1-3, 7, 8 and 18 were rejected under 35 U.S.C. § 102(e) as being anticipated by U.S. Patent Publication No. 2003/01284552 to Chadha in view of U.S. Patent No. 5,636,336 to Adachi; claims 6, 9-12 and 19 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Chadha in view of Adachi and further in view of U.S. Patent No. 5,726,947 to Yamazaki; and claim 20 was rejected under 35 U.S.C. § 103(a) as being unpatentable over Chadha in view of Adachi and further in view of U.S. Patent No. 5,644,758 to Patrick et al. These rejections are traversed with respect to the presently pending claims under rejection, for at least the reasons given below.

Presently pending independent claim 1 now recites, among other things:

wherein said work memory has first and second input ports, said first input port being connected to said graphic engine,

wherein said display memory has third and fourth input ports, said third input port being connected to said second input port, and said fourth input port being connected to a memory controller, and

wherein said data transfer of said first bitmap data from said work memory to said display memory is performed such that a set of data bits of said first bitmap data are transferred at the same time,

wherein said first bitmap data includes a plurality of line data each associated with a line of pixels of an image represented by said second bitmap data to be displayed on said display panel, and

wherein said data transfer of said first bitmap data from said work memory to said display memory is sequentially performed such that each of said line data is transferred in a horizontal period in parallel from said work memory to said display memory.

Based on the above features recited in claim 1, data can be transferred from a work memory to a display memory, and then displayed on a display panel, in a much faster way than what is possible in conventional controller drivers.

In more detail, the capability to *transfer lines of data* ***sequentially*** *from a work memory to a display memory* ***in a horizontal period in parallel*** allows for faster display of image data than what is available through conventional devices.

Turning now to the cited art of record, the Office Action correctly recognizes that Chadha does not teach or suggest the connections among the graphic engine, work memory, display memory, and driver circuit, as claimed, but the Office Action incorrectly asserts that Adachi teaches such features.

In particular, the Office Action asserts that Work Memory Section 48 of Adachi corresponds to the claimed work memory, and has first and second separate ports as claimed. However, this assertion is incorrect. Namely, Work Memory Section 48 has a first input port connected to a transfer processing section 56, and a second input port connected to a various-images processing section 58, as shown in Figure 3 of Adachi. This feature of Adachi does not correspond to the claimed ***work memory that has first and second input ports, with the first input port being connected to a graphic engine***, since neither the transfer processing section 56 nor the various-images processing section 58 of Adachi correspond to a graphic engine.

Still further, Chadha does not teach or suggest that each of a plurality of line data each associated with a line of pixels is transferred at the same time from a work memory to a display memory. In particular, the Office Action asserts that each of the line data is the same as CxRxB byes received at 604. However, this assertion is incorrect. "C" corresponds to the number of columns and "R" corresponds to the number of rows. Thus, the ordinary skilled artisan would understand that the "CxRxB bytes" as image data for only one frame. Therefore, the ordinary skilled artisan would not understand that the "CxRxB bytes" are

transferred at the same time, because the number of bits is too many to be transferred at the same time. Adachi does not rectify this deficiency of Chadha.

In the interest of expediting prosecution, the last "wherein" clause of claim 1 has been amended to make this distinction even more clear, by reciting that the display memory is sequentially performed such that each of the line data is transferred at the same time in a horizontal period in parallel from the work memory to the display memory.

Accordingly, for at least these reasons, presently pending independent claim 1 patentably distinguishes over the combined teachings of Chadha and Adachi.

With respect to dependent claim 7, that claim now recites, among other things:

a memory controller connected to said second input port of said work memory, said memory controller receiving bit map data from a processor for storage in said display memory.

A memory controller that receives bit map data from a processor, for storage in a display memory, are features that are not taught or suggested by the cited art of record.

With respect to dependent claim 12, that claim now recites:

a timing controller controlling said work memory, and said display memory, and said driver circuit,

wherein said driver circuit is connected to said second bit lines, and

wherein said timing controller is adapted to deactivate said display memory to allow said first bitmap data to be transmitted from said work memory to said driver circuit through said second bit lines.

In its rejection of claim 12, the Office Action asserts that column 3, lines 39-44 and Figure 26 of Yamazaki teaches that a controller is adapted to deactivate a display memory to allow first bitmap data to be transmitted from a work memory to a driver circuit through second bit lines. Applicants respectfully disagree with this assertion, since column 3, lines 39-44 of Yamazaki merely describes that a selector selects data, which is then transmitted to a main amplifier. No deactivation of a display memory or any other device is described in this portion of Yamazaki, whereby Figure 26 of Yamazaki also does not show any deactivation of

a display memory. **This deficiency in the prior art has been noted in the last two previously-filed responses, but has not been addressed explicitly in the last two Office Actions.**

Accordingly, presently pending dependent claim 12 is patentable over the cited art of record for these additional reasons, beyond the reasons given above for its base claim.

With respect to dependent claim 18, that claim now recites, among other things:

a memory controller that controls said work memory, said display memory and said driver circuit, said memory controller being ***separate from a processor*** *and being connected to said processor for receiving additional bitmap data to be displayed on said display panel, said additional bitmap data not being stored at any time in said work memory.*

In its rejection of claim 18, the Office Action cites paragraph 0036 and Figure 5 of Adachi for allegedly teaching the claimed memory controller. However, the memory mapped address space is mapped in the micro-controller 200 in the system of Adachi, as explained in paragraph 0036 of Adachi, and **thus the "memory controller" of Adachi is a part of the micro-controller 200 and is not separate from the micro-controller 200**.

Accordingly, presently pending dependent claim 18 is patentable over the cited art of record for these additional reasons, beyond the reasons given above for its base claim.

Dependent claim 20 recites a transferring means and a displaying means, and it also recites that a first rate at which the first bitmap data is transferred from the work memory to the display memory is faster than a second rate at which the second bitmap data is output from the display memory for display on the display panel. In its rejection of claim 20, the Office Action asserts that column 2, lines 1-10 of Patrick teaches the features recited in this claim, but Applicants respectfully disagree.

Namely, column 2, lines 1-10 of Patrick merely describes that the slower the rate of block transfers of data between memory locations, the slower the rate at which a computer system operates, and that block transfers of data between memory locations should be as fast as possible. This says nothing about having one block transfer rate between a first memory and a second memory and having a second block transfer rate (different from the first block transfer rate) between the second memory and another device (e.g., a display). **Rather,**

Patrick would appear to teach having a same, fast transfer rate between all of the devices in his display system, which is totally different from the specific "different speed" features recited in claim 20.

This is essentially the same argument included in the last-filed response, whereby this argument has not been explicitly addressed in the latest Office Action.

Thus, dependent claim 20 patentably distinguishes over the cited art of record for these additional reasons, beyond the reasons given above for its base claim.

Conclusion:

Since all of the issues raised in the Office Action have been addressed in this Amendment and Reply, Applicants believe that the present application is now in condition for allowance, and an early indication of allowance is respectfully requested.

The Examiner is invited to contact the undersigned by telephone if it is felt that a telephone interview would advance the prosecution of the present application.

The Commissioner is hereby authorized to charge any additional fees which may be required regarding this application under 37 C.F.R. §§ 1.16-1.17, or credit any overpayment, to Deposit Account No. 19-0741. Should no proper payment be enclosed herewith, as by a check being in the wrong amount, unsigned, post-dated, otherwise improper or informal or even entirely missing or a credit card payment form being unsigned, providing incorrect information resulting in a rejected credit card transaction, or even entirely missing, the Commissioner is authorized to charge the unpaid amount to Deposit Account No. 19-0741. If any extensions of time are needed for timely acceptance of papers submitted herewith, Applicants hereby petition for such extension under 37 C.F.R. §1.136 and authorize payment of any such extensions fees to Deposit Account No. 19-0741.

Respectfully submitted,

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